

## PATENT COOPERATION TREATY

## PCT

## INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

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Applicant's or agent's file reference 2002-P-105	<b>FOR FURTHER ACTION</b> See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. <b>PCT/KR02/00715</b>	International filing date (day/month/year) 19 APRIL 2002 (19.04.2002)	Priority date (day/month/year) 04 MARCH 2002 (04.03.2002)
International Patent Classification (IPC) or national classification and IPC  <b>IPC7 H01L 21/3065</b>		
Applicant  CI SCIENCE, INC. et al		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 3 sheets, including this cover sheet.
- ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:
- I ☒ Basis of the report
  - II ☐ Priority
  - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
  - IV ☐ Lack of unity of invention
  - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
  - VI ☐ Certain documents cited
  - VII ☐ Certain defects in the international application
  - VIII ☐ Certain observations on the international application

Date of submission of the demand  16 SEPTEMBER 2003 (16.09.2003)	Date of completion of this report  30 DECEMBER 2003 (30.12.2003)
Name and mailing address of the IPEA/KR  Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer  Suh, Tae Jun  Telephone No. 82-42-481-5732 

# INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.

PCT/KR02/00715

## I. Basis of the report

### 1. With regard to the elements of the international application:\*

- ☐ the international application as originally filed
- ☒ the description:  
 pages 1-4, 9-10, , as originally filed  
 pages \_\_\_\_\_, filed with the demand  
 pages 5, 6, 7, 8 , filed with the letter of 18. 12. 2003
- ☒ the claims:  
 pages \_\_\_\_\_, as originally filed  
 pages \_\_\_\_\_, as amended (together with any statement) under Article 19  
 pages \_\_\_\_\_, filed with the demand  
 pages 11 , filed with the letter of 18. 12. 2003
- ☒ the drawings:  
 pages 1/8 - 8/8 , as originally filed  
 pages \_\_\_\_\_, filed with the demand  
 pages \_\_\_\_\_, filed with the letter of \_\_\_\_\_
- ☐ the sequence listing part of the description:  
 pages \_\_\_\_\_, as originally filed  
 pages \_\_\_\_\_, filed with the demand  
 pages \_\_\_\_\_, filed with the letter of \_\_\_\_\_

### 2. With regard to the language, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language English which is

- ☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).
- ☒ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

### 3. With regard to any nucleotide and/or amino acid sequence disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

### 4. ☐ The amendments have resulted in the cancellation of:

- ☐ the description, pages \_\_\_\_\_
- ☐ the claims, Nos. \_\_\_\_\_
- ☐ the drawings, sheet \_\_\_\_\_

### 5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).\*\*

\* Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed." and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).

\*\* Any replacement sheet containing such amendments must be referred to under item I and annexed to this report.

# INTERNATIONAL PATENT EXAMINATION

International application No.

PCT/KR02/00715

## V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

### 1. Statement

Novelty (N)	Claims 1-2	YES
	Claims NONE	NO
Inventive step (IS)	Claims 1-2	YES
	Claims NONE	NO
Industrial applicability (IA)	Claims 1-2	YES
	Claims NONE	NO

### 2. Citations and explanations (Rule 70.7)

#### 1. Reference is made to the following documents:

D1: US 4793975 A (TEGAL CO.)

D2: US 5443689 A (MATSUSHITA ELECTRIC INDUSTRIAL CO.)

#### 2. Novelty (N)

Claims 1-2 relate to electrodes for dry etching a wafer wherein the first electrode including a first flat plate and a ring shaped first protrusion corresponding to one surface of the edge of a wafer and the second electrode including a second flat plate and a ring shaped second protrusion corresponding to other surface of the edge of a wafer.

D1 discloses a lower electrode of a plasma reactor which has a central pedestal which is defined by an annular depression for receiving a wafer and an insert in the shape of a ring for surrounding the pedestal has a raised portion which serves to locate a wafer. The insert comprises an insulator such as ceramic.

D2 discloses a lower electrode which supports a wafer has a recess in its surface and the surface of the electrode is covered with an insulating layer.

D1 and D2 only disclose a lower electrode which have a raised portion on the surface in order to support one surface of a wafer, however, D1 and D2 do not disclose an upper electrode which faces the lower electrode and has a matching protrusion (raised portion) in order to hold the other surface of the wafer, it is apparent that the specific purpose and the proposed configuration of the electrodes for dry etching a wafer disclosed in the present invention through claims 1-2 differ significantly from those in references D1 and D2.

Therefore, the subject matter of claims 1-2 is novel under Article 33(1) and (2).

#### 3. Industrial Applicability (IA)

Claims 1-2 are considered to be industrially applicable.

#### 4. Inventive Steps (IS)

Claims 1-2 relate to a pair of electrodes which face each other wherein the both electrodes include a ring shape protrusion to support the each surface of the edge of a wafer. These features allow the foreign materials deposited on the lower surface of the edge of the wafer to be removed by elevating an electrostatic chuck to bring the upper surface of the edge of the wafer into contact with the protruding part of the first electrode while etching the lower surface of the edge of the wafer.

Although D1 and D2 disclose a lower electrode which has a recess and a raised portion to support one surface of a wafer, the aforementioned features in Claims 1-2 of the present invention, which are required for etching foreign materials deposited on the lower surface of the edge of the wafer, are not disclosed, hence, it is apparent that the invention in claims 1-2 involve an inventive step under Article 33(3) since the subject matter as a whole is neither obvious to the person having ordinary skill in the art nor can it be easily conceived from the technical features disclosed in reference D1 and D2.

Therefore, the claims 1-2 have an inventive step.

the first protrusion and the second protrusion are the same size.

Preferably, an insulation layer may be deposited on or an insulating material may be attached to an inner area of the upper surface of the first electrode, which is inside of the first protrusion.

## 5 Brief Description of the Drawings

The above and other objects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

10 Fig. 1 is a partial cross-sectional view of an electrode for dry etching a semiconductor wafer in accordance with the present invention;

Fig. 2 is a schematic view illustrating the etching of the upper and the side surfaces of a semiconductor wafer using the electrode of the present invention;

Fig. 3 is a schematic view illustrating the etching of the lower and the side surfaces of the semiconductor wafer using the electrode of the present invention;

15 Fig. 4 is a cross-sectional view of a dry etching device provided with the electrode of the present invention;

Fig. 5 is a side view of semiconductor wafer, on which multiple layers are deposited;

20 Fig. 6 is a schematic view illustrating the attachment of foreign materials on the semiconductor wafer by equipment.

Figs. 7a to 7e are cross-sectional views illustrating a process for removing a nitride layer using a conventional wet etching;

Figs. 8a to 8e are cross-sectional views illustrating a process for removing a poly-silicon layer using a conventional dry etching; and

25 Fig. 9 is a schematic view illustrating the etching of a semiconductor wafer using a conventional electrode.

Best Mode for Carrying Out the Invention

Fig. 1 is a partial cross-sectional view of an electrode for dry etching a semiconductor wafer in accordance with the present invention. The electrode of the present invention comprises a pair of electrodes, i.e., a first electrode 10 and a second electrode 20. The first electrode 10 and the second electrode 20 are means for generating plasma for removing foreign materials deposited and accumulated on the edge of the semiconductor wafer.

Herein, the first electrode 10 is used as an anode and the second electrode 20 is used as a cathode. However, the first electrode 10 may be used as a cathode and the second electrode 20 may be used as an anode.

10 The same as the conventional electrode, the first electrode 10 is shaped as a flat circle. A ring-shaped first protrusion 10a is formed on the bottom surface of the first electrode 10. A gas inlet hole 10b is formed between the first protrusion 10a and the circumference of the first electrode 10. The gas inlet hole 10b serves to introduce a reactive gas for generating plasma into a vacuum chamber (not shown), in which the first electrode 10 and the second electrode 20 are formed.

20 The second electrode 20 is also shaped as a flat circle having the same diameter of that of the first electrode 10. An opening 20a is formed on the center of the second electrode 20 and a ring-shaped second protrusion 20b having the same dimension as that of the first protrusion 10a is formed between the opening 20a and the circumference of the second electrode 20.

25 A flat portion of the outside of the first protrusion 10a of the first electrode 10 and a flat portion of the outside of the second protrusion 20b of the second electrode 20 are referred to as a first flat portion 10c and a second flat portion 20c.

30 An insulation layer or an insulator 11 is deposited on or attached to an inner area of the bottom surface of the first protrusion 10a. The attached insulating material 11 serves to prevent an electric field or an electromagnetic field from being formed between the first electrode 10 and the second electrode 20, when a RF power is supplied between the first electrode 10 and the second electrode 20. Polyimide, Teflon, silicon, quartz, or ceramic may be used as the

insulator 11.

Figs. 2 and 3 illustrate the etching of a semiconductor wafer using the electrode of the present invention. Hereinafter, with reference to Figs. 2 and 3, an interaction between the first and the second electrodes 10, 20 of the present invention and the semiconductor wafer 30 is described.

As shown in Fig. 2, the semiconductor wafer 30 is interposed between the first electrode 10 as the anode and the second electrode 20 as the cathode by an electrostatic chuck 40. The electrostatic chuck 40 is installed at a lowering position via the opening 20a of the second electrode 20, thereby bringing the lower surface 30c of the edge of the semiconductor wafer 30 into contact with the upper surface of the second protrusion 20b of the second electrode 20.

A reactive gas is introduced via the gas inlet hole 10b of the first electrode 10 and power is supplied from the RF generator 50 to the second electrode 20, thereby forming an electric field or an electromagnetic field through the first protrusion 10a and the first flat portion 10c of the first electrode 10 and the second protrusion 20b and the second flat portion 20c of the second electrode 20. Then, two types of plasma with different intensity are generated by the reactive gas between the first protrusion 10a and the second protrusion 20b and between the first flat portion 10c and the second flat portion 20c.

Herein, plasma is formed along width of the first protrusion 10a and the second protrusion 20b. The width of the first protrusion 10a and the second protrusion 20b corresponds to the width B of the edge of the semiconductor wafer 30 to be etched. Therefore, an area A of the semiconductor wafer 30, in which fine circuit pattern 31 is formed, is not affected by this plasma. The side surface 30b of the semiconductor wafer 30 is etched by plasma C formed between the first flat portion 10c and the second flat portion 20c.

Since the lower surface 30c of the semiconductor wafer 30 is in contact with the upper surface of the second protrusion 20b of the second electrode 20, the etching is mainly performed on the upper surface 30a and the side surface 30b of the semiconductor wafer 30 by RIE (Reactive Ion Etching).

Further, since the insulating material 11 attached to the inner area of the

first electrode 10, an electric field or an electromagnetic field is not formed in the area A, thereby preventing plasma from being generated on the area A and improving the efficiency of the etching.

Herein, reference number 60 denotes a matching network.

5 As shown in Fig. 3, the electrostatic chuck 40 is elevated via the opening 20a of the second electrode 20, thereby bringing the upper surface 30a of the edge of the semiconductor wafer 30 into contact with the upper surface of the first protrusion 10a of the first electrode 10. Then, the reactive gas is introduced via the gas inlet hole 10b of the first electrode 10 and the power is supplied from the  
10 RF generator 50, thereby generating plasma between the first protrusion 10a and the second protrusion 20b. Herein, the etching is mainly performed on the lower surface 30c and the side surface 30b of the semiconductor wafer 30 by plasma, thereby removing the foreign materials deposited on the area B.

Fig. 4 is a cross-sectional view of a vacuum chamber 70, in which the  
15 electrode of the present invention is installed. The vacuum chamber 70 comprises a blow pipe 71 for introducing a reactive gas for generating plasma into the first electrode 10 and the second electrode 20, a port 70a for entering the semiconductor wafer 30, an outlet 70b for exhausting the gas after the etching of the semiconductor wafer 30, and the electrostatic chuck 40 for moving the  
20 semiconductor wafer 30 upward and downward.

The semiconductor wafer 30 is entered into the vacuum chamber 70 via the port 70a and mounted on the electrostatic chuck 40. Under a reactive gas atmosphere, the RF generator 50 supplies a voltage via the second electrode 20. At this time, the upper surface of the central portion of the semiconductor wafer 30  
25 is protected by the insulating material 11 of the first electrode 10, and plasma is generated between the first protrusion 10a and the second protrusion 20b and between the first flat portion 10c and the second flat portion 20c. Then, the upper, the lower, and the side surfaces 30a, 30c, and 30b of the edge of the semiconductor wafer 30 are etched through the aforementioned process.

30 During the etching process, the same as the conventional case, the foreign materials removed from the semiconductor wafer 30 and the reactive gas are

## Claims:

- 5 1. An electrode for dry etching a wafer, said electrode comprising a first electrode and a second electrode for removing foreign materials from the edge of the wafer by plasma, said first electrode including a first flat plate and a ring-shaped first protrusion corresponding to one surface of the edge of a wafer, and said second electrode including a second flat plate and a ring-shaped second protrusion corresponding to the other surface of the edge of the wafer, wherein said first protrusion and said second protrusion are the same size.
- 10 2.(amended) The electrode for dry etching a wafer as set forth in claim 1, wherein an insulation layer is deposited on or an insulating material is attached to an inner area of the upper surface of the first electrode, which is inside of the first protrusion.